CLEAN VERSION OF PENDING CLAIMS

63. (Amended) A microelectronic structure comprising:

a substrate;

a gate electrode formed over the substrate and defining an underlying channel region in the substrate, said gate electrode having a barrier layer formed on a sidewall of the gate electrode to prohibit the silicidation of the sidewall;

a source/drain extension formed in the substrate adjacent the gate electrode and having a first silicide layer formed therein; and

a source/drain region formed in the substrate adjacent the source/drain extension and having an activated doped region with a second silicide layer disposed therein, the activated doped region and the second silicide layer are aligned with a spacer disposed along sidewalls of the gate electrode, said second silicide layer formed after removing a portion of said barrier layer formed over a top surface of the gate electrode, said source/drain extension having less dopant concentration than the activated doped region, and the source/drain extension and the first silicide layer are aligned with the gate electrode to have the less dopant concentration of the extension reside between the channel region and the activated doped region.

64. (Amended) The microelectronic structure of claim 63, wherein the activated doped region is thicker than the source/drain extension.

65. (Amended) The microelectronic structure of claim 63, wherein the second silicide layer is thicker than the first silicide layer.

66. (Amended) The microelectronic structure of claim 63, wherein the activated doped region and the source/drain extension comprise ion implanted material.

67. The microelectronic structure of claim 63, wherein the first and second silicide layers comprise different metals.

68. The microelectronic structure of claim 63, wherein the first and second silicide layers comprise a same metal.

69. The microelectronic structure of claim 63, wherein the second silicide layer comprises $CoSi_2$.

70. The microelectronic structure of claim 63, wherein the second silicide layer comprises $TiSi_2$.

71. (Amended) The microelectronic structure of claim 63, wherein the second silicide layer comprises nickel silicide.

72. The microelectronic structure of claim 63, wherein the first silicide layer comprises $CoSi_2$.

73. The microelectronic structure of claim 63, wherein the first silicide layer comprises $TiSi_2$.

74. (Amended) The microelectronic structure of claim 63, wherein the gate electrode having a third silicide layer formed on the top surface of the gate electrode.

75. (Amended) The microelectronic structure of claim 63, wherein the barrier layer comprises silicon nitride.

76. (Amended) The microelectronic structure of claim 63, wherein the source/drain extension is approximately 300-500 angstroms in thickness.

77. (Amended) A source, drain and gate structure comprising:

a semiconductor substrate;

a gate electrode formed over the substrate semiconductor and defining an underlying channel region in the substrate, said gate electrode having a barrier layer formed on a sidewall of the gate electrode to prohibit the silicidation of the sidewall;

a source/drain extension formed in the substrate adjacent the gate electrode and having a first silicide layer formed therein; and

a source/drain region formed in the substrate adjacent the source/drain extension and having an activated doped region with a second silicide layer disposed therein, the activated doped region and the second silicide layer are aligned with a spacer disposed along sidewalls of the gate electrode, said gate electrode having a third silicide layer formed on a top surface of the gate electrode, said second and third silicide layers formed after removing a portion of said barrier layer formed over the top surface of the gate electrode, said source/drain extension having less dopant concentration than the activated doped region, and the source/drain extension and the first silicide layer are aligned with the gate electrode to have the less dopant concentration of the extension reside between the channel region and the activated doped region.

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78. (Amended) The microelectronic structure of claim 77, wherein the activated doped region is thicker than the source/drain extension.

79. (Amended) The microelectronic structure of claim 77, wherein the second silicide layer is thicker than the first silicide layer.

80. (Amended) The microelectronic structure of claim 77, wherein the activated doped region and the source/drain extension comprise ion implanted material.

81. The microelectronic structure of claim 77, wherein the first and second silicide layers comprise different metals.

82. The microelectronic structure of claim 77, wherein the first and second silicide layers comprise a same metal.

83. The microelectronic structure of claim 77, wherein the second silicide layer comprises $CoSi_2$.

84. The microelectronic structure of claim 77, wherein the second silicide layer comprises $TiSi_2$.

85. (Amended) The microelectronic structure of claim 77, wherein the second silicide layer comprises nickel silicide.

86. The microelectronic structure of claim 77, wherein the first silicide layer comprises $CoSi_2$.

87. The microelectronic structure of claim 77, wherein the first silicide layer comprises $TiSi_2$.

88. (Amended) The microelectronic structure of claim 77, wherein the second and third silicide layers comprise a same metal.

89. (Amended) The microelectronic structure of claim 77, wherein the barrier layer comprises silicon nitride.

F 5 Cont

90. (Amended) The microelectronic structure of claim 77, wherein the source/drain extension is approximately 300-500 angstroms in thickness.